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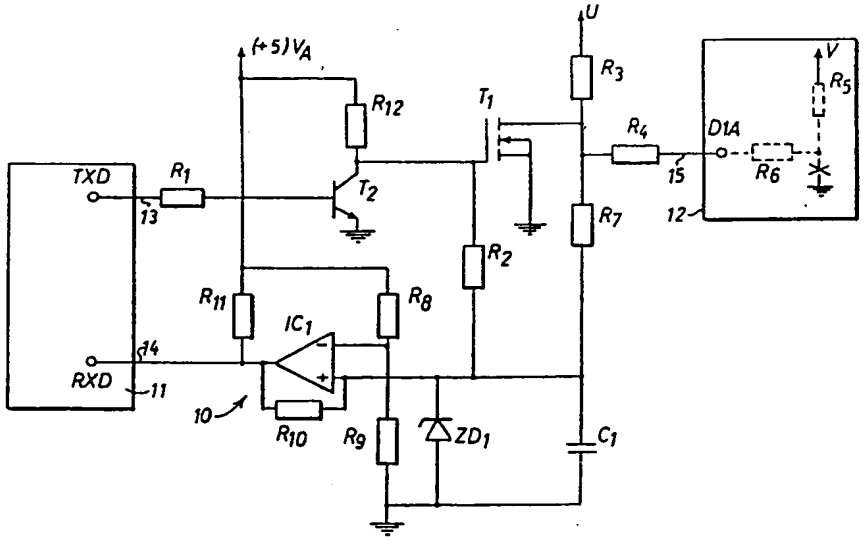
(54) Title: AN INTERFACE FOR USE BETWEEN TWO COMMUNICATION UNITS



(57) Abstract

An interface for use between a first communication unit having a two-wire connection and a second communication unit having a single-wire connection includes a comparator (IC1) having a fixed potential ($V_{(-)}$) at its inverting input and has its output connected to one of the two-wire connections whilst the potential ($V_{(+)}$) applied to the non-inverting input is determined by a switching network (transistors T1 and T2 and resistors R2, R3, R4, R7, R12) responsive to the potential on the second of the two-wire connections and on the single-wire connection to enable the first communication unit to receive data from the second communication unit but not receive self-transmitted data.

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DESCRIPTION

AN INTERFACE FOR USE BETWEEN TWO COMMUNICATION UNITS.

State of the Art

The present invention relates to an interface for use between two communication units in accordance with the first part of claim 1. Such communication units may form part of a device used in the control of a fuel system of an internal combustion engine in response to monitoring exhaust gas composition; the first communication unit having a two-wire connection may be a micro-computer and the second communication unit having a single-wire connection part of the monitoring system.

It is known to control the fuel-to-air ratio of an internal combustion engine in response inter alia to the composition of the results of the exhaust gas with a view to reduction in air pollution, and frequently catalytic oxidation is adapted in order to substantially avoid the discharge into the atmosphere of carbon monoxide resulting from incomplete combustion of the fuel. To this end the exhaust gas is analysed by measurement of its thermal conductivity and its composition expressed as the percentage of carbon dioxide present. With micro-computer control of the fuel system there is a need for supplying to the micro-computer signals characterising the instantaneous actual composition and the corresponding desired composition of the exhaust gas as well as other engine performance parameters. The nature of these signals as regards their levels, input and output impedances and their frequency of transmission have been established by ISO specifications.

When the micro-computer is in a position to transmit data to a communications partner it is desirable that it should be able to do so without delay and a conventional two-wire interface involving

direct connection between two wires can result in the computer receiving self-transmitted data which is undesirable for echo suppression.

Advantages of the invention

An interface in accordance with the characterising part of claim 1, overcomes the disadvantage of a conventional two-wire to two-wire interface and facilitates rapid transmission of data by the micro-computer whilst at the same time preventing reception of self-transmitted data.

In particular by forming the switching network with the transistors and a plurality of resistors in accordance with the feature of claim 5, the potential at the output of the comparator can be made dependent upon the potentials on one of the two-wire connections of the first communications unit which can be a micro-computer and of the single-wire connection of the communications partner.

Drawing

The invention will be further described by way of example, with reference to the accompanying drawing, which is a circuit diagram of an interface according to a preferred embodiment of the invention.

The interface 10 whose circuit is shown in the drawing is for connecting a first communications unit 11 such as a micro-computer requiring a two-wire interface to a second communication unit or partner 12 for which a single-wire interface would be suitable. In normal operation when the first communication unit 11 transmits no data a pin TXD is at a high potential whereas when the first communication unit 11 transmits data, the pin TXD is at low potential and data is transmitted from that pin. When the communication partner 12 is inactive a pin DIA is at a high potential and when the communication unit 12 has data to transmit is at a low potential and data is

transmitted from that pin. Transmitted data can be received by the communication unit 11 on pin RXD when at a low potential.

In the interface 10, leads 13 and 14 comprise the first and second of the two-wire connections to the communication unit 11, and the lead 15 is the single-wire connection to the second communication unit 12. A resistor R1 connects lead 13 to the base of a transistor T2 whose emitter is connected to ground and whose collector is connected to a source V_A through a resistor R12. The collector of the transistor T2 is connected via a resistor R2 to the non-inverting input of a comparator IC1. A predetermined potential is applied to the inverting input of the comparator IC1 by the potential divider formed by resistors R8 and R9 connected between the source V_A and ground. The output of the comparator IC1 is connected to the source V_A through resistor R11 and to the non-inverting input through a resistor R10. The output of the transistor T2 at the collector is connected to the gate of FET transistor T1 whose source is connected through a resistor R3 to a voltage source V_B and through a resistor R4 to the lead 15 which forms the single-wire connection to a pin DIA of the communication partner 12. The conditions existing inside the communication partner 12 with regard to the potential of the pin DIA are illustrated diagrammatically by a resistor R6 which can be connected to a source illustrated as V_B through a resistor R5 or to ground. The junction between resistors R3 and R4 is extended to the non-inverting input of the comparator IC1 through the resistor R7, and a Zener diode ZD1 and a capacitor C1 are connected between the non-inverting input and ground for stabilization.

The potential $V_{(-)}$ at the inverting input of the comparator IC1 is set by V_A and resistors R8 and R9, but the potential $V_{(+)}$ at the non-inverting input of the comparator IC1 depends upon whether the pin TXD is at a high or low potential and whether the pin DIA is at a high or low potential. Three conditions may be considered as follows:

1. When the communication unit 11 is inactive or does not transmit any data the pin TXD is at a high potential so that transistor T_2 is switched through and the end of the resistor R2 remote from the non-inverting input of the comparator IC1 is effectively connected to ground and the potential at the non-inverting input is determined by the voltage divider formed on the one hand by resistor R2 and on the other hand resistor R7 in series with the parallel combination of resistor R3 and resistors R4, R5, R6 connected between V_B and ground, V_A can be conveniently 5 volts and V_B can vary between 6 and 50 volts and the values of the resistances of the resistors can be chosen so that when V_B is as low as 6 volts the potential at the non-inverting input $V_{(+)}$ of the comparator IC1 will be greater than the potential $V_{(-)}$ at the inverting input so that the output of the comparator IC1 will be at a high potential so that the lead 14 keeps pin RXD at a high potential to prevent it receiving data.

2. When the communications unit 11 transmits data the pin TXD is at a low potential and this blocks transistor T2 which enables transistor T1 to switch through, and the potential $V_{(+)}$ at the non-inverting input of the comparator IC1 is determined by the potential divider formed by resistors R12, R2 and R7 connected between source V_A and ground. The potential $V_{(+)}$ can then still be higher than that $V_{(-)}$ at the inverting input so that the output of the comparator

IC1 will remain at high potential thereby maintaining pin RXD at high potential and preventing the reception of self-transmitted data.

3. When the communication partner 12 transmits data the pin DIA is at a low potential. If at this time pin TXD is at a high potential the transistor T2 is switched through and one end of resistor R2 is effectively connected to ground. Resistors R3, R4 and R6 form a potential divider connected between V_B and ground, and a fraction of the potential at the junction of resistors R3 and R4 is applied to the non-inverting input of the comparator IC1 by the voltage divider formed by resistors R7, R2 and R12. By suitable choice at the values of resistors this potential $V_{(+)}$ can be very much less than the potential $V_{(-)}$ at the inverting input, even when V_B is as high as 50 volts, so that the output of the comparator IC1 is then at a low potential and the pin RXD of the communication unit 11 is held at a low potential so that data transmitted from the communication partner 12 can be received in the communication unit 11.

By way of example in a preferred embodiment the transistor T1 is a BC848, the transistor T2 is a BSS123, the comparator IC1 is an LM2901, Zener diode ZD1 is a Z6V8, V_A is 5 volts and V_B 6-50 volts; and the resistances of the various resistors are as follows:

R1	1 kohm
R2	100 ohm
R3	100 kohm
R4	100 ohm
R5	100 kohm
R6	100 ohm
R7	100 khom

R8	56 kohm
R9	10 kohm
R10	464 kohm
R11	2 kohm
R12	2.7 kohm

and the capacitor C1 0.1 nF.

With these components the potential at the inverting input of the comparator IC1 is as follows:

$$V_{(-)} = \frac{R9}{R8 + R9} \times V_A = 0{\cdot}75V$$

under the first conditions when the pin TXD is at a high potential, the potential at the non-inverting input of the comparator is as follows:

$$V_{(+)} = \frac{R2}{R2 + (R3 \,||\, (R4 + R5 + R6)) + R7} \times V_B = \frac{1}{6} V_B$$

so that with V_B at the minimum of 6 volts $V_{(+)} = 1$ volt.

Under the second conditions when pin TXD is at a low potential, the potential $V_{(+)}$ at the non-inverting input of the comparator IC1 is as follows:

$$V_{(+)} = \frac{R7}{R7 + R12 + R2} \times V_A = 3.75V$$

$V_{(+)}$ is therefore greater than $V_{(-)}$, namely 0.75v, and the output of the comparator is at a high potential.

Under the third conditions when pin DIA is at a low potential and pin TXD is at a high potential, the potential $V_{(+)}$ at the non-inverting input of the comparator IC1 is as follows:

$$V_{(+)} = \frac{R4 + R6}{R3 + R4 + R6} \times \frac{R2}{R7 + R2} \times V_B = \frac{1}{2000} \cdot V_B$$

when V_B is at its maximum of 50 volts the potential $V_{(+)}$ at the non-inverting input of the comparator IC1 is 23mV which is less than the potential $V_{(-)}$ at the non-inverting input and the output of the comparator is at a low potential which is applied to the terminal RXD to enable it to receive data.

A particular advantage of an interface embodying the present invention is that of echo suppression since it will be appreciated that the data transmitted by the communications unit 11 on pin TXD are not simultaneously received by the micro-computer on pin RXD. In the 8051 family of micro-computers, the transmitting process is initiated as soon as data is sent to a transmitting register and the actual transmitting process subsequently takes place automatically without having to be controlled by software. With a conventional interface the program has to be interrupted in order to wait until the transmitting process has ended and the subsequent clearing of the receiving register where data transmitted a short time previously has been stored frees the receiving register in order to be able to receive data arriving externally. Such waiting time which is thereby necessitated can accumulate very rapidly if several data transmissions take place each time a program is run since a program cannot be completed during the waiting time and any time critical program sequences can be inacceptably delayed.

CLAIMS

1. An interface for use between a first communication unit having a two-wire connection and a second communication unit having a single-wire connection, characterised by a comparator whose output is extended to a first of the two-wire connections and has its non-inverting input extended to the single-wire connection for transmitting data signals from the second communications unit to the first communications unit, a transistor connected to the second of the two-wire connections, and a switching network responsive to the high/low potential of the second of the two-wire connections and the high/low potential of the single-wire connection for controlling transmission through said transistor and for controlling the potential of the non-inverting input of the comparator, whereby when a data signal is transmitted by the first communications unit on the second of the two-wire connections the output of the comparator is at high potential and the first of the two-wire connections is at high potential so that the data transmitted by the first communications unit is not received by the first communications unit on the first of the two-wire connections and when a data signal is transmitted by the second communications unit on the single-wire connection the output of the comparator is at low potential and such transmitted data is received by the first communications unit on said first of the two-wire connections.

2. An interface as claimed in claim 1, in which the switching network includes a second transistor (T2) responsive to the potential of the second (TXD) of the two-wire connections (TXD, RXD).

3. An interface as claimed in claim 2, in which the first transistor is a field-effect transistor (T1)

and the output of the second transistor (T2) is connected to the gate thereof and to the non-inverting input of the comparator (IC1) which is also extended to the single-wire connection (DIA).

4. An interface as claimed in claim 3, in which said switching network comprises said first and second transistors and a plurality of resistors interconnected to serve as a series of potential dividers determining the potential applied to the non-inverting input of the comparator (IC1), and of which potential dividers a first (R2, R3, R4, R5, R6, R7) is between a first source (V_B) and ground and is effective when the first (TXD) of the two-wire connections is at a high potential, a second (R2, R7, R12) is between a second source (V_A) and ground and is effective when the first (TXD) of the two-wire connections is at low potential, and a third (R2, R3, R4, R5, R7) is between the first source (V_B) and ground and is effective when the single-wire connection (DIA) is at low potential.

5. An interface as claimed in claim 4, in which the first potential divider is established when the second transistor (T2) is switched through, in which the second potential divider is established by the first transistor is switched through, and the third potential divider is established when the single-wire connection is at low potential.

6. An interface as claimed in any preceding claim, in which a predetermined potential is applied to the inverting input of the comparator (IC1) by a further potential divider (V_A: R8, R9), and the non-inverting input of the comparator (IC1) is stabilised by a diode (ZD1) and a capacitor (C1) connected to ground.

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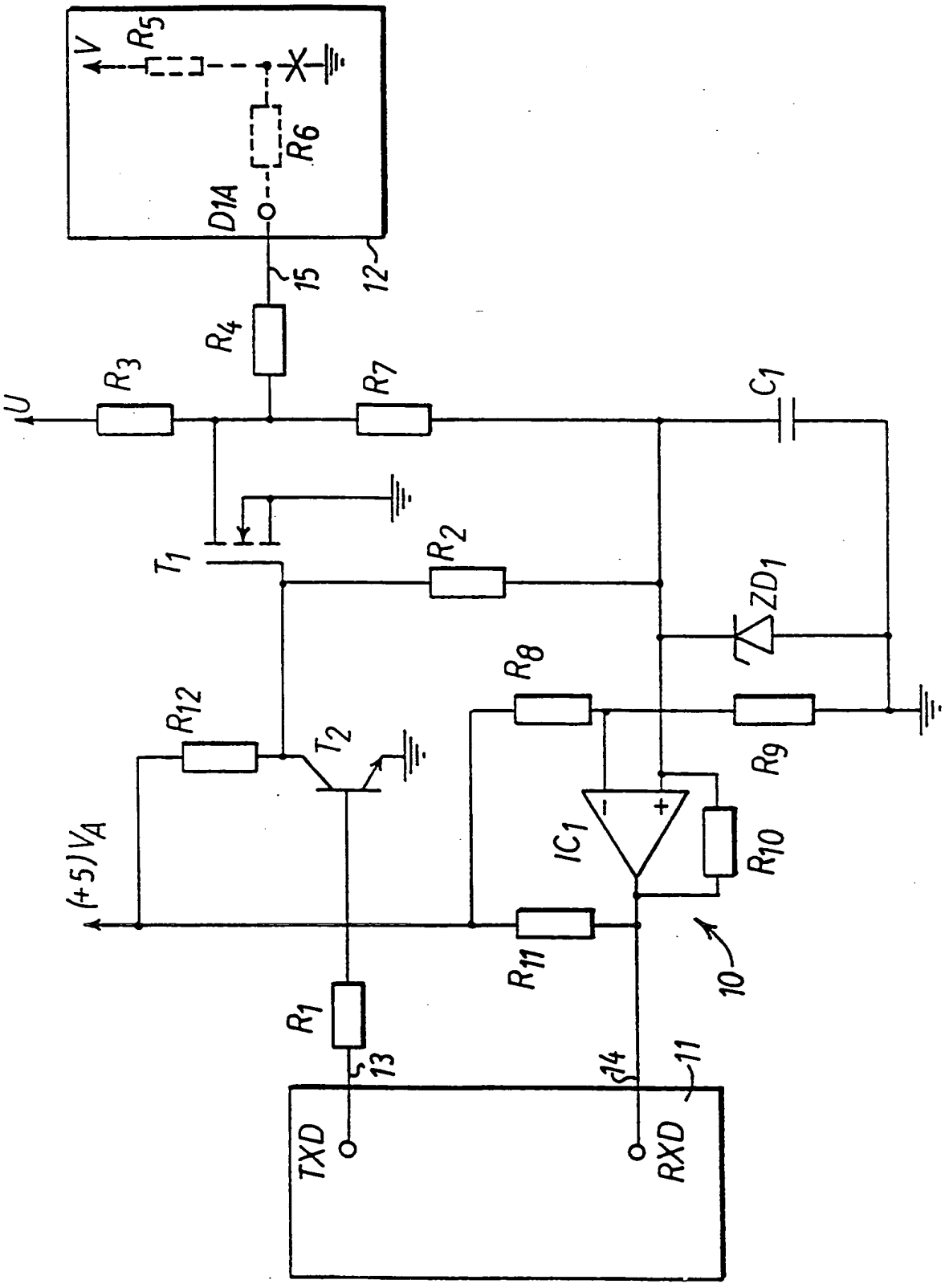
V
R5
R6
D1A
15
12
R4
R3
R7
U
C1
T1
R2
ZD1
R8
R12
T2
R9
IC1
R10
(+5) VA
R11
10
R1
13
14
11
TXD
RXD

INTERNATIONAL SEARCH REPORT

International Application No PCT/EP 88/00904

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC4: H 04 L 5/16

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System [8]	Classification Symbols
IPC4	H 04 B; H 04 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [9]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	DE, C2, 3029054 (PHILIPS PATENTVERWALTUNG GMBH) 17 July 1986, see column 4, line 24 - column 7, line 24; figures 1-2 --	1-6

* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
24th May 1989	16 JUN 1989

International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. PCT/EP 88/00904

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-C2- 3029054	17/07/86	GB-A-B- 2082876	10/03/82
		JP-A- 57053167	30/03/82
		FR-A-B- 2493644	07/05/82
		US-A- 4419752	06/12/83